

Figure 1
programmable
logic device 10

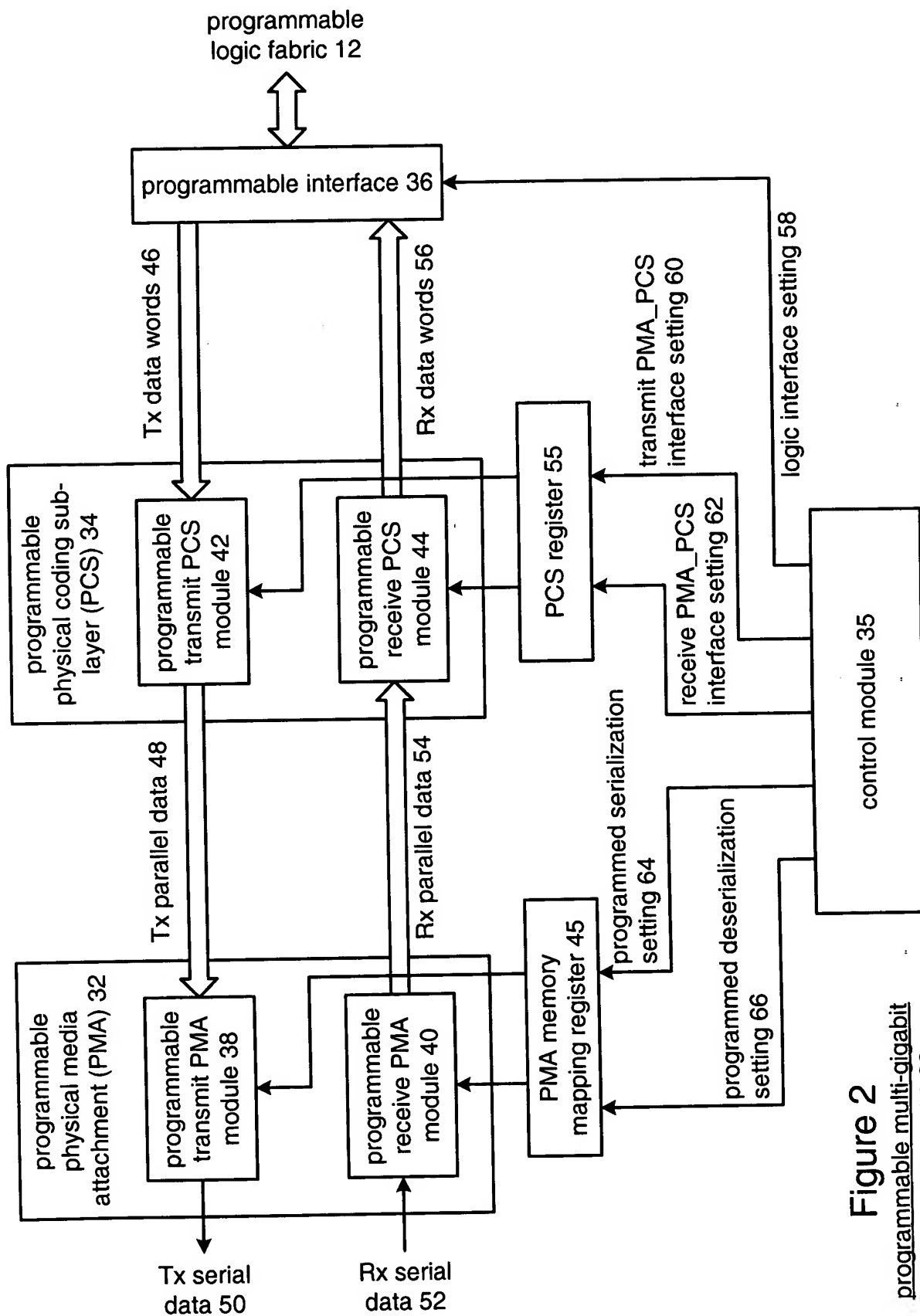


Figure 2
programmable multi-gigabit
transceivers 14-28

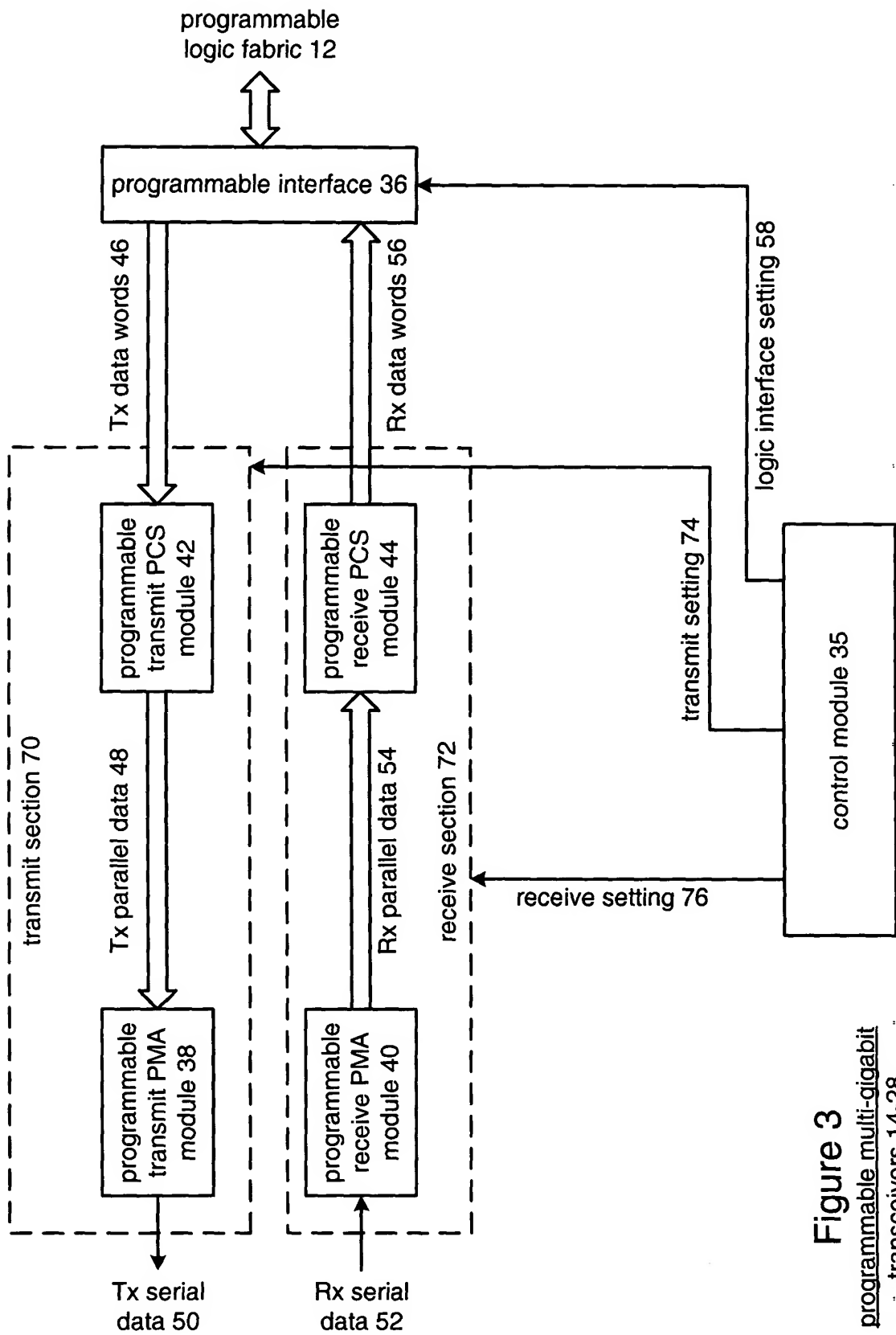


Figure 3
programmable multi-gigabit
transceivers 14-28

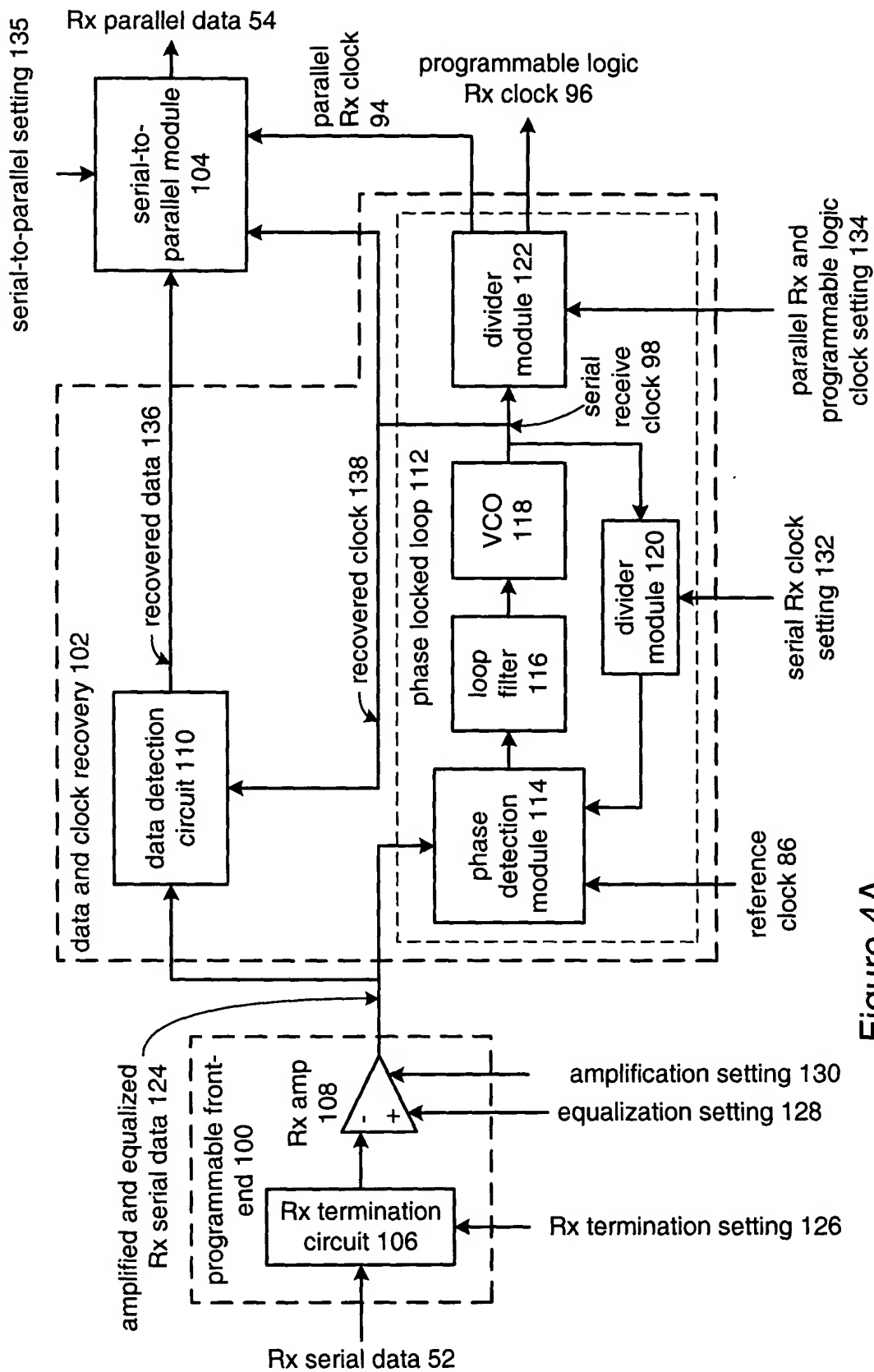


Figure 4A
 programmable receive
 PMA module 40

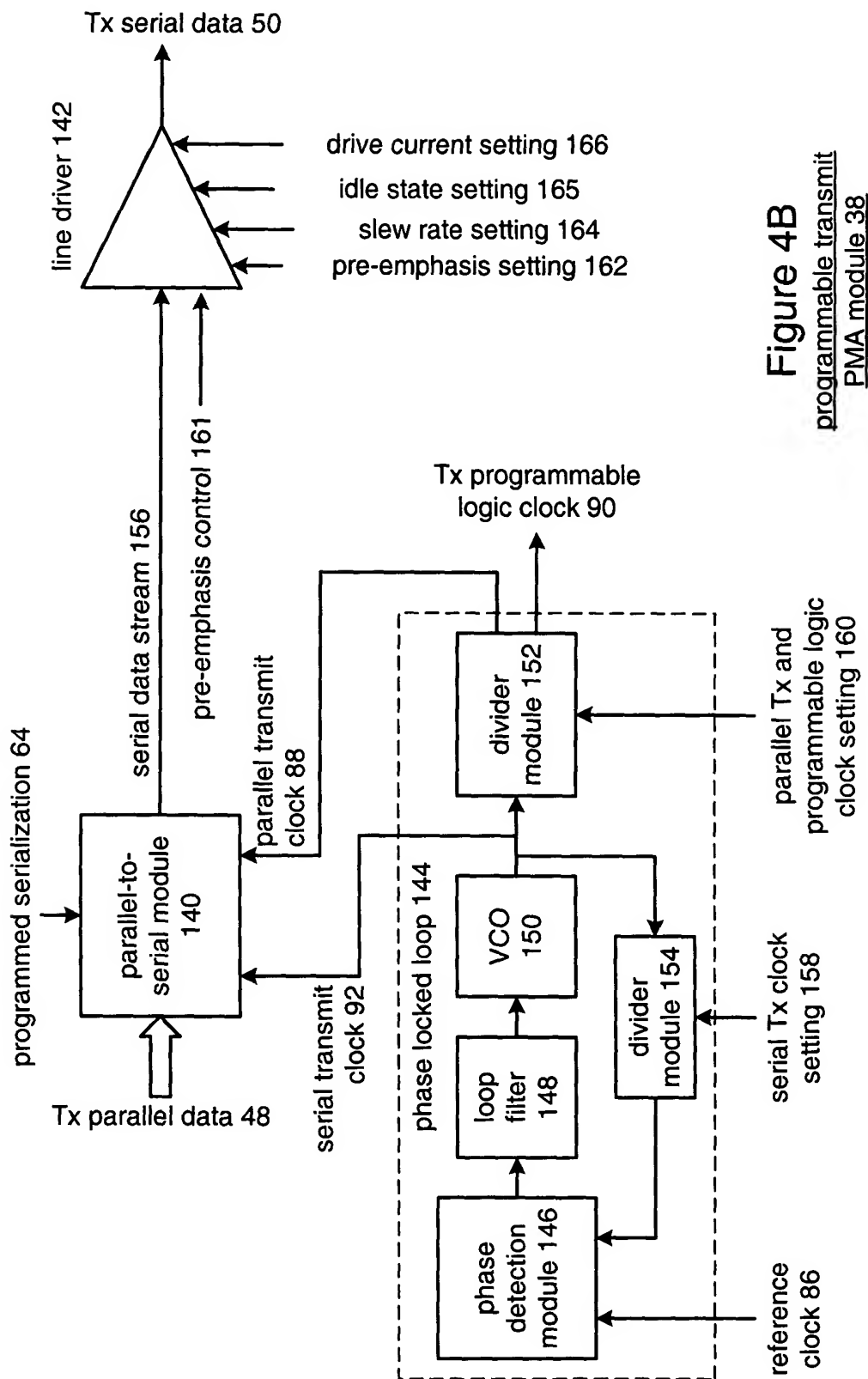


Figure 4B
programmable transmit
PMA module 38

user selected mode	description
00	automatic (default)
01	lock to local reference for data sampling operations
10	lock to received data
11	reserved

Figure 6
PLL 170 operation

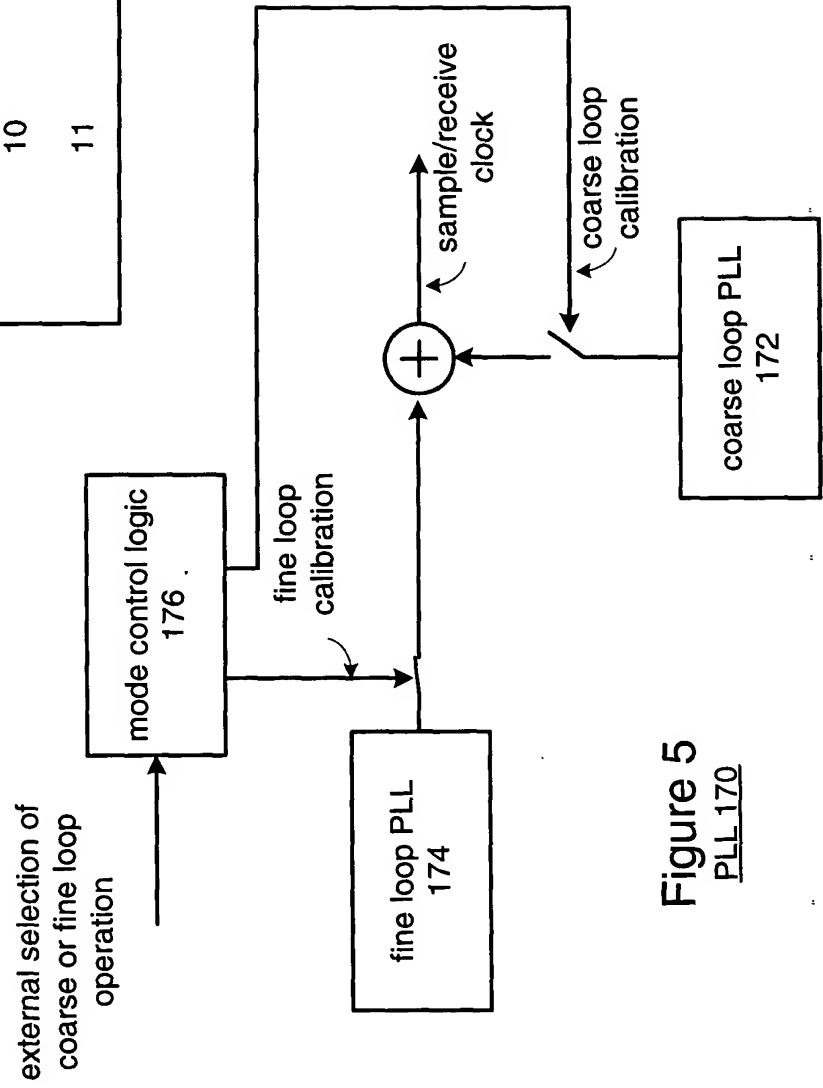


Figure 5
PLL 170

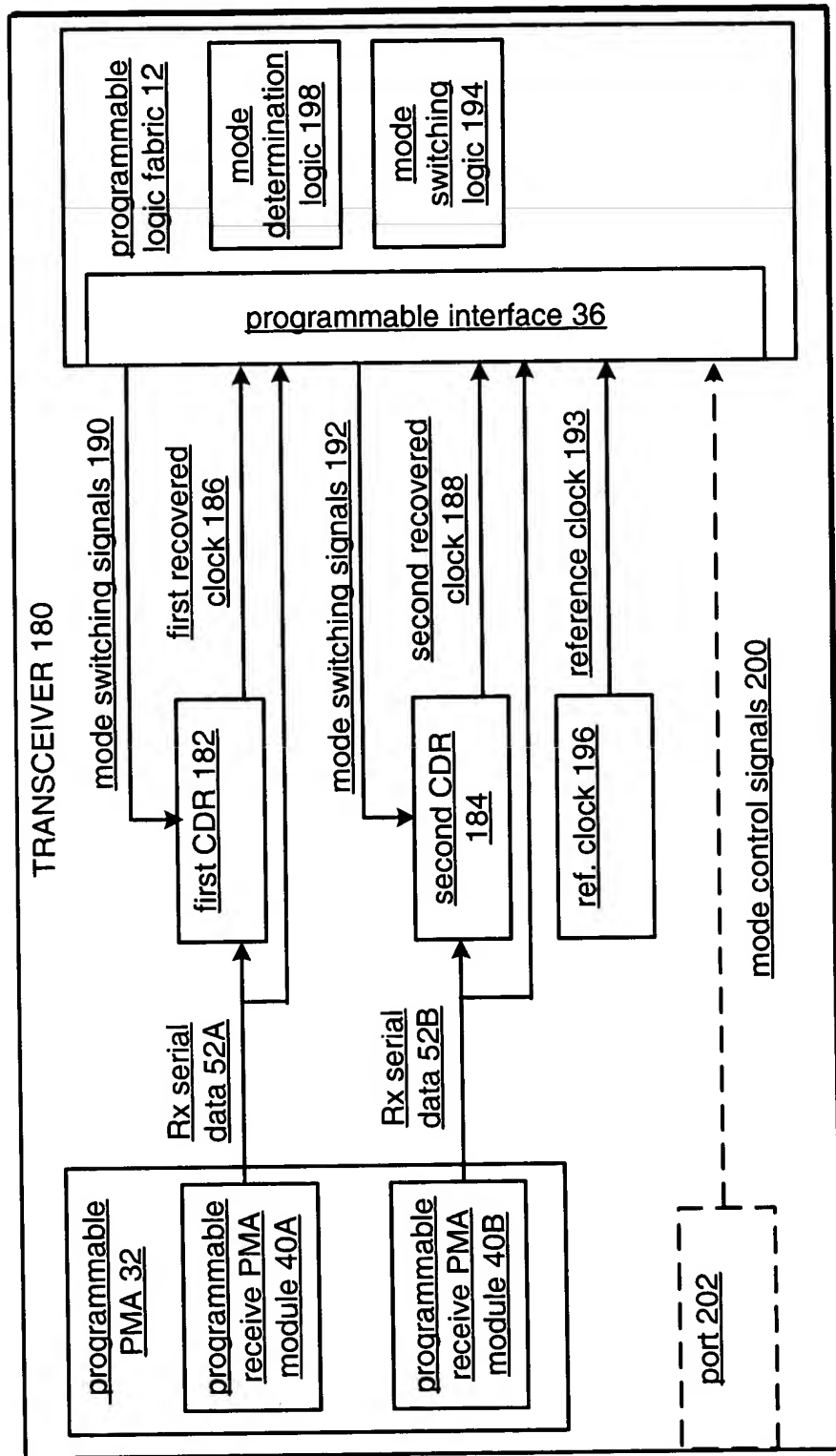


Figure 7
transceiver 180

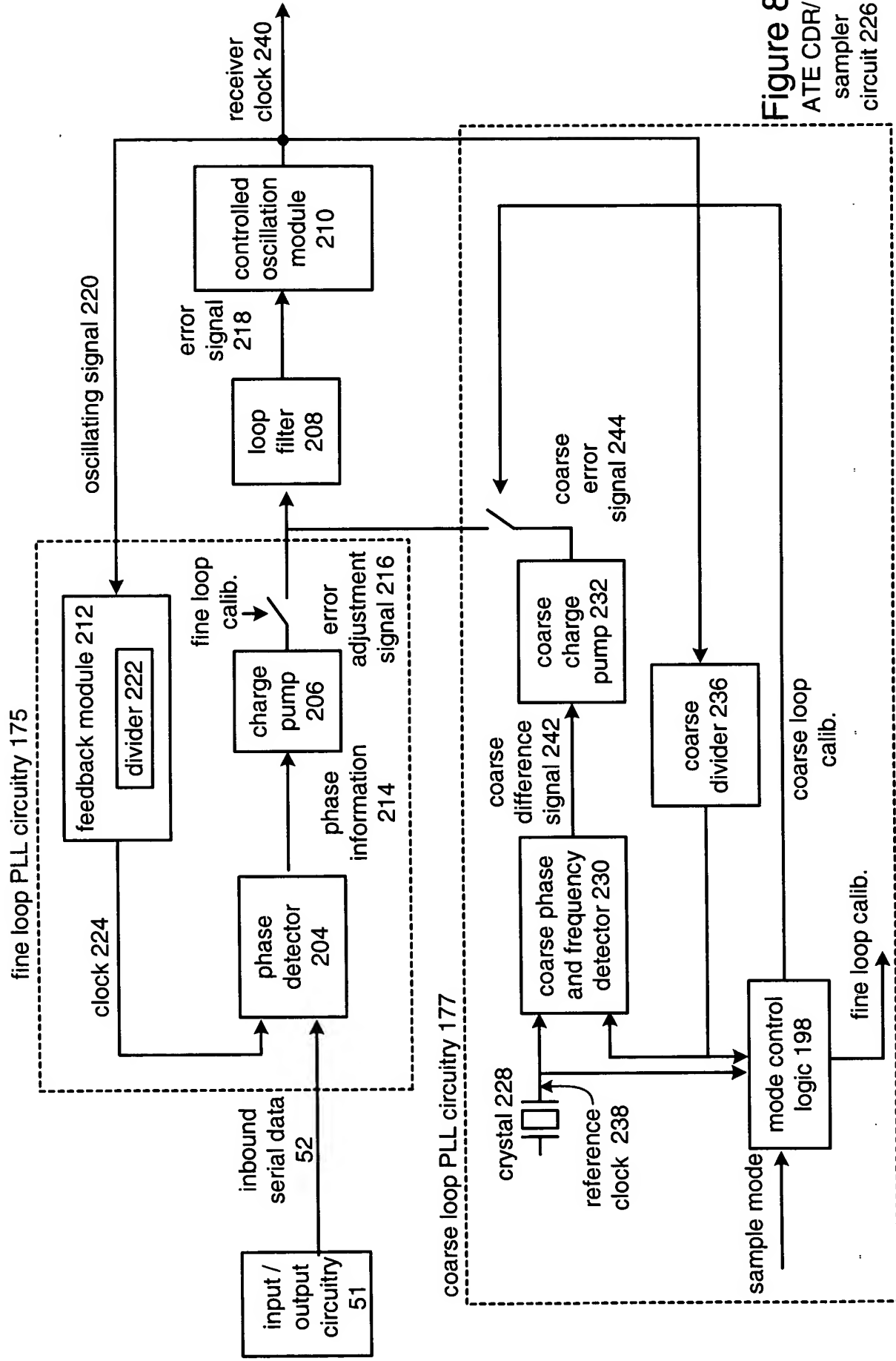


Figure 8
ATE CDR/
sampler
circuit 226

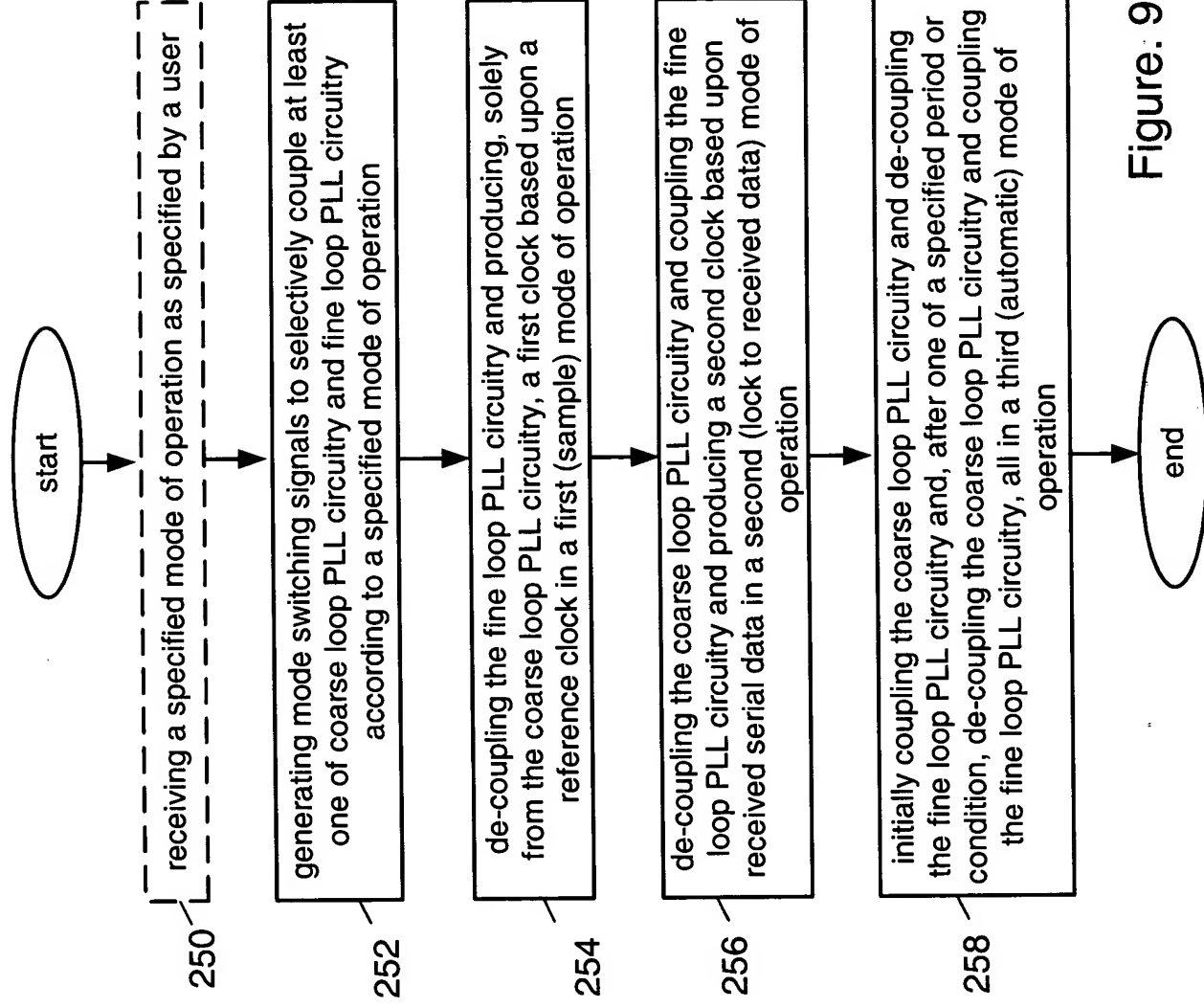


Figure: 9